CLAIMS

What is claimed is:

1. An emulation logic board designed for circuit emulation, comprising

a plurality of input/output (I/O) pins;

a plurality of emulation integrated circuits (IC) having reconfigurable logic resources and reconfigurable interconnect resources; and

on-board data processing resources coupled said emulation ICs to locally generate and apply first configuration signals to configure selected ones of said reconfigurable logic resources of said emulation ICs to be used to emulate a partition of an IC design, and second configuration signals to configure selected ones of said reconfigurable interconnect resources of said emulation ICs to interconnect said selected ones of said reconfigurable logic resources of said emulation ICs, responsive to external emulation requests received through said I/O pins.

2. The emulation logic board as set forth in claim 1, wherein the on-board data processing resources comprise

storage medium having stored therein programming instructions designed to operate the emulation logic board to perform said local generation and application of configuration signals to configure said selected ones of said reconfigurable logic and interconnect resources of said emulation ICs, and

a processor coupled to the storage medium to execute said programming instructions.

3. The emulation logic board as set forth in claim 1, wherein said on-board data processing resources further receive through said I/O pins said partition of an IC design, and locally determine interconnect routing within said selected ones of said reconfigurable logic resources of said emulation ICs to be used to emulate said partition of an IC design.

4. The emulation logic board as set forth in claim 3, wherein the on-board data processing resources comprise

storage medium having stored therein programming instructions designed to operate the emulation logic board to perform said local determination of routing within said selected ones of said reconfigurable logic resources of said emulation ICs, and

a processor coupled to the storage medium to execute said programming instructions.

5. The emulation logic board as set forth in claim 1, wherein at least one of said emulation ICs comprises on-chip data processing resources to cooperate and assist said on-board data processing resources to perform said local generation and application of configuration signals.

6. The emulation logic board as set forth in claim 5, wherein

said on-board data processing resources further receive through said I/O pins said partition of an IC design, and locally determine interconnect routing within said selected ones of said reconfigurable logic resources of said emulation ICs to be used to emulate said partition of an IC design; and

at least one of said on-chip data processing resources of said at least one emulation IC further cooperates and assists said on-board data processing resources to perform said local determination of interconnect routing within said selected ones of said reconfigurable logic resources of said emulation ICs to be used to emulate said partition of an IC design.

7. In an emulation apparatus, a method of operation comprising:

locally generating on an emulation logic board, using on-board data processing resources, first configuration signals to configure selected ones of reconfigurable logic resources of emulation ICs of said emulation logic board to emulate a partition of an IC design;

locally generating on said emulation logic board, using said on-board data processing resources, second configuration signals to configure selected ones of reconfigurable interconnect resources of said emulation ICs to interconnect said selected ones of reconfigurable logic resources of said emulation ICs; and

applying said first and second configuration signals to configure said selected ones of said reconfigurable logic and interconnect resources of said emulation ICs of said emulation logic board.

8. The method as set forth in claim 7, wherein at least one of said local generation of first and second configuration signals is at least partially performed in conjunction with on-chip data processing resources of at least one of said emulation ICs of said emulation logic board.

9. The method as set forth in claim 7, wherein the method further comprises

receiving said partition of an IC design through a plurality of input/output (I/O) pins of the emulation logic board; and

locally determining by said on-board data processing resources of said emulation logic board, interconnect routing within said selected ones of said reconfigurable logic resources of said emulation ICs of said emulation logic board.

10. The method as set forth in claim 9, wherein at least one of said local determination of interconnect routing is at least partially performed in conjunction with on-chip data processing resources of at least one of said emulation ICs of said emulation logic board.

11. An emulation system comprising:

a workstation including electronic design automation (EDA) software to partition an integrated circuit (IC) design into a plurality of partitions; and

an emulator including a plurality of logic boards, coupled to said workstation, each of said logic boards having a plurality of emulation ICs and on-board data processing resources, and each of said emulation ICs having reconfigurable logic and interconnect resources, wherein each of the on-board data processing resources include logic to correspondingly and distributively generate configure signals to configure selected ones of said reconfigurable logic and interconnect resources of its emulation ICs, to facilitate emulation of said IC design, responsive to emulation requests of said EDA software.

12. The emulation system as set forth in claim 11, wherein the on-board data processing resources comprise

storage medium having stored therein programming instructions designed to operate the emulation logic board to perform said local generation and application of configuration signals to configure said selected ones of said reconfigurable logic and interconnect resources of said emulation ICs of said emulation logic board, and

a processor coupled to the storage medium to execute said programming instructions.

13. The emulation system as set forth in claim 11, wherein said on-board data processing resources further receive said partition of an IC design from said EDA software, and locally determine interconnect routing within said selected ones of said reconfigurable logic resources of said emulation ICs of said emulation logic board to be used to emulate said partition of an IC design.

14. The emulation system as set forth in claim 13, wherein the on-board data processing resources comprise

storage medium having stored therein programming instructions designed to operate the emulation logic board to perform said local determination of routing within said selected ones of said reconfigurable logic resources of said emulation ICs of said emulation logic board, and

a processor coupled to the storage medium to execute said programming instructions.

15. The emulation system as set forth in claim 11, wherein at least one of said emulation ICs comprises on-chip data processing resources to cooperate and assist said on-board data processing resources of said emulation logic board to perform said local generation and application of configuration signals.

16. The emulation system as set forth in claim 15, wherein

said on-board data processing resources of said emulation logic board further receive said partition of an IC design from said EDA software, and locally determine interconnect routing within said selected ones of said reconfigurable logic resources of said emulation ICs to be used to emulate said partition of an IC design; and

at least one of said on-chip data processing resources of said at least one of said emulation ICs of said emulation logic board further cooperates and assists said on-board data processing resources of said emulation logic board to perform said local determination of interconnect routing within said selected ones of said reconfigurable logic resources of said emulation ICs of said emulation logic board to be used to emulate said partition of an IC design.

17. An emulation apparatus comprising:

a plurality of collections of reconfigurable logic and interconnect resources; and

a plurality of groups of data processing resources correspondingly coupled to said collections of reconfigurable logic and interconnect resources to correspondingly and distributively generate configuration signals to configure selected ones of reconfigurable logic and interconnect resources to emulate circuit elements of corresponding partitions of an IC design.

18. The emulation apparatus as set forth in claim 17, wherein at least one group of the data processing resources comprises storage medium having stored therein programming instructions designed to perform said corresponding and distributive

generation of configuration signals, and a processor coupled to the storage medium to execute the programming instructions.

19. The emulation apparatus as set forth in claim 17, wherein at least one group of the data processing resources further correspondingly and distributively determine interconnect routing for selected ones of the corresponding collection of reconfigurable logic resources.

20. The emulation apparatus as set forth in claim 19, wherein at least one group of data processing resources comprises storage medium having stored therein programming instructions designed to perform said corresponding and distributed determination of interconnect routing.

21. A method comprising:

partitioning an integrated circuit (IC) design to be emulated into a number of partitions; and

correspondingly and distributively generating configuration signals to configure selected ones of reconfigurable logic and interconnect resources of corresponding collections of reconfigurable logic and interconnect resources, to emulate corresponding partitions of said partitioned IC design.

22. The method as set forth in claim 21, wherein the method further comprises correspondingly and distributively determining interconnect routing for said selected ones of reconfigurable logic and interconnect resources of said corresponding collections of reconfigurable logic and interconnect resources.

23. An emulation integrated circuit (IC) comprising:

a plurality of reconfigurable logic and interconnect resources; and

on-chip data processing resources coupled to said reconfigurable logic and interconnect resources to locally generate configuration signals to configure selected ones of said reconfigurable logic and interconnect resources of said emulation IC to emulate circuit elements of a partition of an IC design.

24. The emulation IC as set forth in claim 23, wherein said on-chip data processing resources comprises storage medium having stored therein programming instructions designed to perform said local generation of configuration signals, and a processor coupled to the storage medium to execute the programming instructions.

25. The emulation IC as set forth in claim 23, wherein said on-chip data processing resources further locally determine interconnect routing within said selected ones of said reconfigurable logic resources of said emulation IC.

26. The emulation IC as set forth in claim 25, wherein said on-chip data processing resources comprises storage medium having stored therein programming instructions designed to perform said local determination of interconnect routing.

27. In an emulation integrated circuit (IC), a method of operation comprising:

locally generating on said emulation IC, using on-chip data processing resources, first configuration signals to configure selected ones of reconfigurable logic resources of the emulation IC to emulate a partition of an IC design;

locally generating on said emulation IC, using said on-chip data processing resources, second configuration signals to configure selected ones of reconfigurable interconnect resources of said emulation IC to interconnect said selected ones of reconfigurable logic resources of said emulation IC; and

applying said first and second configuration signals to configure said selected ones of said reconfigurable logic and interconnect resources of said emulation IC.

28. The method as set forth in claim 27, wherein the method further comprises locally determining by said on-chip data processing resources of said emulation IC, interconnect routing within said selected ones of said reconfigurable logic resources of said emulation IC